A NEW WDF THREE-PORT ADAPTOR SUITABLE FOR FLOATING-POINT ARITHMETIC AND/OR DSP IMPLEMENTATIONS

Xiaojian Liu *Leonard T. Bruton*

Department of Electrical and Computer Engineering
The University of Calgary, Calgary Alberta
Canada T2N 1N4

ABSTRACT

A new decomposed version of three-port adaptors for wave digital filters (WDFs) is proposed, which is especially suitable for floating-point arithmetic and for implementation on digital signal processors (DSPs). By using the proposed three-port adaptor, the concept of modified wave digital filters (MWDFs) is appropriately extended to WDFs involving any n-port adaptors (n is integer). The resulting MWDFs preserve all the important properties of WDFs, in particular, those relating to stability.

1. INTRODUCTION

Wave digital filters (WDFs) [1] possess a number of excellent high-performance properties [2] such as low coefficient sensitivity and various types of stability under finite wordlength conditions. All these good properties result from the losslessness and passivity of the WDF building blocks, in particular, the WDF adaptors.

Under finite wordlength conditions, an adaptor is made passive if all arithmetic operations inside the adaptor are carried out exactly by means of appropriately extended signal wordlengths inside the adaptor, i.e., the behavior of the adaptor is so-called conditionally linear. This concept is suitable for special-purpose hardware implementations using fixed-point arithmetic. However, for implementations using a commercial digital signal processor (DSP), the signal wordlength is predetermined and the user is not able to extend the internal signal wordlength without significant computational overhead. Therefore, these DSP implementations present a type of problem that is not encountered when designing custom hardware. Moreover, ensuring the passivity under finite wordlength conditions has been a general problem with respect to floating-point arithmetic, because the method of extending internal wordlength becomes infeasible for floating-point additions, if the operands have very different exponents. In this contribution, we are concerned with implementation methods that can solve these problems and thereby facilitate DSP and/or floating-point implementations.

Most commercial fixed-point DSPs have two interesting properties. First, they possess an accumulator with double (or longer) signal wordlength. Second, the computing combination of 1 multiplication and 1 accumulation can be performed in 1 cycle either inherently or by using pipelining. By making use of the first property, WDF adaptors can be made strictly passive [3]. However, the number of processing cycles required for computing the outputs of an n-port adaptor is in this case n^2, which is larger than the minimum possible $4n - 6$ (for the case of elementary adaptors [4]).

In order to reduce the number of computing cycles to the minimum, while maintaining the passivity property of adaptors, modified wave digital filters (MWDFs) have been proposed [5] for WDFs involving just two-port adaptors. In the approach [5], the second of the above stated DSP's properties is appropriately employed. Also, the MWDFs in [5] are suitable for floating-point implementations.

As is known [4], WDFs require for implementation, in general, two elementary adaptors, which are the two-port adaptor and the three-port adaptor having a reflection-free port. Thus, there is a need to extend the concept of MWDFs in [5] to the case of three-port adaptors. To this end, we propose an appropriate extension in this paper.

To extend the MWDFs to the case of three-port adaptors, the approach in [5] should not be used directly, because the direct extension mentioned in [5] cannot retain all the passivity properties of WDFs, in particular, the incremental passivity property [5], which is related to the forced-response stability and other related properties [6,7]. Moreover, an appropriate extension is more important to implementations using floating-point arithmetic, because for the direct extension of [5] it is even not known how to effectively guarantee the simple passivity under finite wordlength conditions, which is related particularly to the freedom from limit cycle oscillations. Recall that any floating-point digital filter that cannot be built strictly without parasitic oscillations can always sustain a parasitic oscillation involving the highest possible value of the exponent [8,9].

In this contribution, we propose a new three-port adaptor which overcomes all the above mentioned problems. It enables us to achieve MWDFs which possess all the well-known desirable sensitivity and stability properties of WDFs, while the number of DSP processing cycles remains minimal. Although the number of multiplications in the proposed MWDF three-port adaptor is not minimal compared with the voltage-wave digital filter (VWDF) three-port adaptor, the new adaptor is also important for floating-point special-purpose hardware implementations because it ensures passivity under floating-point

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arithmetic, which is especially suitable for implementing MWDFs [10].

2. DECOMPOSITION OF THE THREE-PORT ADAPTOR

The proposed three-port adaptor is a decomposed version of the conventional three-port adaptor. This decomposed three-port adaptor is comprised of 3 equal-structured two-port building blocks. Thus, the original three-port problem is reduced to a combined two-port problem.

The decomposed versions of three-port adaptors have been used for various purposes [11,12]. Although all the decomposed three-port adaptors are equivalent, i.e., they realize the same scattering matrix describing the adaptor, the internal structures, in particular, the interconnections of the two-port building blocks, may be quite different, in order to suit the specific applications.

Further, it can be shown that power-wave digital filters (PWDFs) and voltage-wave digital filters (VWDFs) result in the same MWDFs. We focus hereafter on PWDFs and will give a more comprehensive discussion elsewhere.

It is known [2] that the scattering matrix describing an n-port adaptor (n is an integer greater than 1) used in PWDFs is an orthogonal matrix. By using Given's algorithm [13], any orthogonal matrix can be decomposed into products of elementary orthogonal matrices, each corresponding to a planar rotation [2]. Using this property, we can decompose a three-port adaptor into 3 two-port building blocks.

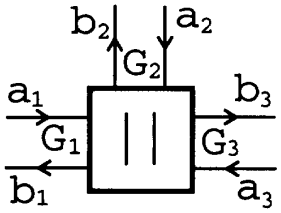

Figure 1. Symbol of the three-port parallel adaptor

2.1. Three-Port Parallel Adaptor

2.1.1. Unconstrained Three-Port Parallel Adaptor

The conventional unconstrained three-port parallel adaptor given in Fig.1 is described by the scattering matrix $\mathbf{S}_p$ and

$$\mathbf{b}=\mathbf{S}_p\mathbf{a} \text{ with } \mathbf{S}_p=\begin{pmatrix} \gamma_1^2-1 & \gamma_1\gamma_2 & \gamma_1\gamma_3 \\ \gamma_2\gamma_1 & \gamma_2^2-1 & \gamma_2\gamma_3 \\ \gamma_3\gamma_1 & \gamma_3\gamma_2 & \gamma_3^2-1 \end{pmatrix}, \quad (1a,b)$$

where $\mathbf{a}=(a_1,a_2,a_3)^T$, $\mathbf{b}=(b_1,b_2,b_3)^T$ (the superscript T denotes the transpose) and $\gamma_i=\sqrt{2G_i/G_0}$ (G_i is the port conductance at the port i.). With $G_0=G_1+G_2+G_3$ and then $\gamma_1^2+\gamma_2^2+\gamma_3^2=2$, $\mathbf{S}_p$ is orthogonal.

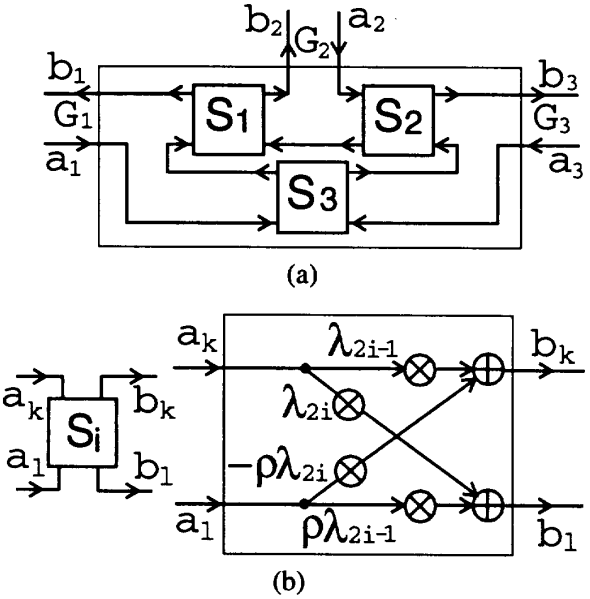

Figure 2. (a) Decomposed three-port adaptor. (b) Two-port building block

The decomposition of $\mathbf{S}_p$ in (1b) can be given by

$$\mathbf{S}_p=\begin{pmatrix} \lambda_1 & -\rho\lambda_2 & 0 \\ \lambda_2 & \rho\lambda_1 & 0 \\ 0 & 0 & 1 \end{pmatrix}\begin{pmatrix} 1 & 0 & 0 \\ 0 & \lambda_3 & -\rho\lambda_4 \\ 0 & \lambda_4 & \rho\lambda_3 \end{pmatrix}\begin{pmatrix} \lambda_5 & 0 & -\rho\lambda_6 \\ 0 & 1 & 0 \\ \lambda_6 & 0 & \rho\lambda_5 \end{pmatrix}, \quad (2a)$$

where the integer ρ is unimodular and $\rho=1$ for the parallel adaptor.

After carring out the matrix multiplications in (2a) and the comparison of the entries in (1b) and (2a), we obtain the equivalence of (1b) and (2a) by setting

$$\begin{aligned} &\lambda_4=\rho\gamma_2\gamma_3, \quad \lambda_3=\pm\sqrt{1-\lambda_4^2} \\ &\lambda_5=\frac{\rho(\gamma_3^2-1)}{\lambda_3}, \quad \lambda_6=\frac{\gamma_1\gamma_3}{\lambda_3} \\ &\lambda_1=\frac{\gamma_2^2-1}{\lambda_3}, \quad \lambda_2=\frac{-\gamma_1\gamma_2}{\lambda_3}. \end{aligned} \quad (2b)$$

It can be seen, by using the relations below (1), that

$$\lambda_1^2+\lambda_2^2=\lambda_3^2+\lambda_4^2=\lambda_5^2+\lambda_6^2=1, \quad (3)$$

which verifys that the plane rotation matrices are orthogonal. Defining the submatrices $\mathbf{S}_i$ ($i=1,2,3$) as follows

$$\mathbf{S}_i=\begin{pmatrix} \lambda_{2i-1} & -\rho\lambda_{2i} \\ \lambda_{2i} & \rho\lambda_{2i-1} \end{pmatrix}, \quad (4)$$

we obtain the signal block diagram in Fig.2 for the decomposed three-port parallel adaptor. The corresponding signal flow graph does not contain any directed loops and therefore it is realizable.

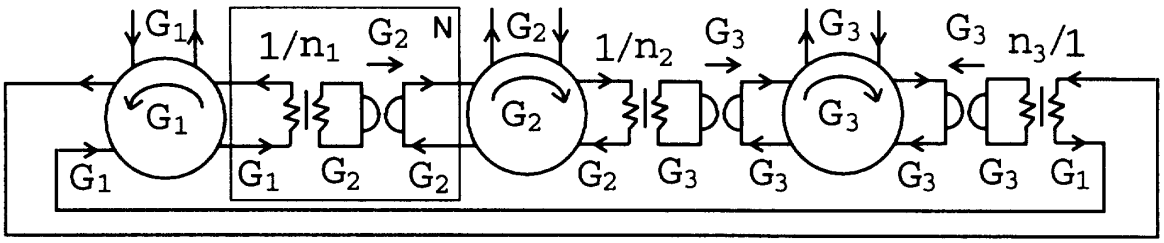

Figure 3. Reference-domain circuit of the decomposed three-port parallel adaptor

It is well-known from classical network theory that the two-port scattering matrix $\mathbf{S}_i$ can be realized by using an ideal transformer and eventually a gyrator. Taking into account the interconnections between the blocks $\mathbf{S}_i$ in Fig.2a, we obtain the overall reference-domain circuit for the decomposed three-port adaptor in Fig.3.

2.1.2. Reflection-Free Three-Port Parallel Adaptor

The three-port adaptor with a reflection-free port is one of the two elementary adaptors. Without loss of generality, we choose the port 3 to be the reflection-free port, i.e., $G_3 = G_1 + G_2$. This results in $\gamma_3 = 1$ or equivalently $\lambda_5 = 0$. The corresponding signal block diagram is given in Fig.4, where the single sign-inverter can be absorbed in the block $\mathbf{S}_1$.

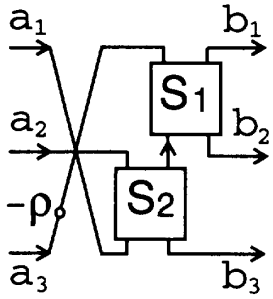

Figure 4. Decomposed reflection-free three-port adaptor

2.2. Three-Port Series Adaptor

For PWDFs, the scattering matrices of the parallel adaptor, $\mathbf{S}_p$, and the series adaptor, $\mathbf{S}_s$, are formally related by

$$\mathbf{S}_p = -\mathbf{S}_s, \tag{5}$$

where the entries of $\mathbf{S}_s$ are however defined by $\gamma_i = \sqrt{2R_i/R_0}$ with $R_i = 1/G_i$, $R_0 = R_1 + R_2 + R_3$ and $R_3 = R_1 + R_2$ for the reflection-free adaptor. Therefore, all the decomposition relations discussed above for the parallel adaptors hold formally for the series adaptors with the unimodular constant $\rho = -1$. This also means that, for the reference-domain circuit of the decomposed three-port series adaptor, there are no gyrators present.

2.3. On the Decomposed Adaptors

Let us reconsider Fig.2. By decomposition, the lossless three-port adaptor is partitioned into 3 lossless two-port blocks $\mathbf{S}_1$ to $\mathbf{S}_3$, each of which realizes an ideal transformer, a gyrator and a two-port adaptor. To compute one output value of such a two-port block, it requires 2 multiplications and 1 addition which is to be carried out at last. Thus, the nonlinear operations, such as truncations and overflow corrections, can be performed immediately after the addition or they can be integrated with the addition. In other words, the addition is not required to be performed exactly. This property is most important for floating-point arithmetic, where additions cannot be performed exactly in many situations.

Because the multiplications can be carried out exactly by using double precision for output signals in both fixed-point and floating-point arithmetic, and taking into account the considerations in the last paragraph, the two-port blocks $\mathbf{S}_i$ can be made conditionally linear for both types of arithmetic. Thus, the passivity of the overall three-port adaptor is guaranteed.

The number of multiplications in the two-port block $\mathbf{S}_i$, which is 4, can be reduced to 2 by appropriate scaling. The scaling procedure must obey certain conditions. That is, the resultant multiplication coefficients must not be greater than unity in magnitude. Further, the final scaled WDF, which involves multiple three-port adaptors, should consist of two-port blocks containing only 2 multiplications, each of which is combined with an accumulation, enabling the efficient use of the above-mentioned second property of DSPs. Also, no multipliers should be left outside the two-port blocks except at the input and output. In fact, the scaled WDF is the so-called MWDF.

The final scaled unconstrained WDF three-port adaptor has 6 multiplications combined with 6 accumulations. The scaled reflection-free three-port adaptor has 4 multiplications combined with 4 accumulations. This results in 6 and 4 computing cycles, respectively, which are also the minimum number of computing cycles for VWDF three-port adaptors.

3. SCALING, QUANTIZATION AND STABILITY

The scaling and coefficient quantization procedure of the decomposed three-port adaptor is different from that of the two-port adaptor. As can be expected, these procedures are more complicated for the three-port adaptor, even though the final result is quite simple.

3.1. Scaling

The scaling procedure for the three-port adaptor is recursive. A number of simple linear relations have to be satisfied. In particular, there are 8 possible scaling strategies for the decomposed reflection-free three-port adaptor and 24 possible scaling strategies for the decomposed unconstrained three-port adaptor. It is shown that among these possible strategies, *there always exists one for which all the multiplication coefficients are not greater than unity in magnitude.* A searching algorithm for this desired result is given.

3.2. Coefficient Quantization

In most cases, the two-port block $\mathbf{S}_i$ cannot be made lossless under the finite coefficient wordlength condition. In order to make the two-port block at least passive, several possible quantization conditions are given. Among these conditions, there is one which imposes the least restrictions on the coefficients.

First, it is easy to make the decomposed WDF three-port adaptor shown in Figs.2 and 4 passive, because, according to (3) and (4), it is necessary and sufficient to ensure

$$\lambda_{2i-1}^2 + \lambda_{2i}^2 \leq 1, \quad i = 1, 2, 3. \tag{5}$$

That is, the procedure of coefficient quantizations can be carried out independently for each of the WDF two-port blocks $\mathbf{S}_i$.

However, the coefficient quantization procedures for the scaled MWDF building blocks are not anymore independent of each other. In many cases (in particular, when a port of the adaptor is interconnected with a shift element), the coefficient quantization conditions for each building block within a decomposed MWDF adaptor are related to each other. Also, an appropriate quantization order has to be given.

A set of sufficient quantization conditions and an appropriate quantization order are given, which are easy to be satisfied.

3.3. Stability

By using the decomposed three-port adaptor, all the stability and related properties of conventional WDFs under finite wordlength conditions can be ensured by using the same means, that is, magnitude truncations and saturations for signal under- and overflow corrections.

4. SIMULATION

A computer simulation example has been completed, which shows that a conventional three-port adaptor cannot be made passive; that is, parasitic oscillations occur if the minimum number of computing cycles is required for implementations on DSPs. However, by using the proposed decomposed three-port adaptor, the passivity and the minimum number of computing cycles are guaranteed.

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