In most signal applications such as conversion and detection, $I \gg I$, for a good quality device. Hence,

$$T_{eq} \cong \frac{\eta T}{2}, \text{ K}.$$  (5)

To verify the effect of $\eta$ on the noise of high-frequency diodes, several devices with different values of $\eta$ were selected and measured at high frequency. The measurement frequency of 60 MHz with a noise bandwidth of several megahertz was chosen so that the measurement would not include any $1/f$ noise. The measurement method is basically a switched radiometer and is discussed in detail elsewhere [5].

Fig. 1 shows the effect of the ideality factor on the equivalent noise temperature of forward-biased diodes. Units A, B, and C are silicon Schottky barriers, while units D and E are GaAs Schottky barrier diodes. Unit F is a n-n Ge-Si heterojunction. The experimental points are obtained at the value of current, which results in the minimum equivalent noise temperature (Fig. 2). The theoretical curve is obtained from (5).

It should be noted that if the leakage currents, series resistance, or high-frequency conductance were taken into account in the theoretical curve, there would be an even better fit between theory and experiment.

Fig. 2 shows the noise of three Schottky-barrier diodes, measured at 60 MHz, versus the dc bias current. This figure illustrates the minimum in the equivalent noise temperature at a value of forward-biased current. It also illustrates the effect of $R_s$ at higher current levels. The contribution of the thermal noise of $R_s$ to the total noise becomes significant when the junction resistance becomes comparable to $R_s$. It should also be noted that the closer $\eta$ is to unity and the smaller $R_s$, the larger the current range over which a desirable noise characteristic is obtained.

In conclusion, the ideality factor is directly related to the minimum noise temperature of a diode and can be used as a selection criterion for low-noise diodes. The closer $\eta$ is to one, the lower the minimum equivalent noise temperature. The reduction in $\eta$ can only be accomplished by taking greater care with the metallurgical variables during fabrication. In addition, the series resistance should be minimized in order to minimize the noise at higher current levels. Once a diode has been chosen for a given application, the value of the dc bias current must be considered in order to obtain a minimum equivalent noise temperature.

REFERENCES

A Voltage-Tuned Gyrator

L. T. BRUTON

Abstract—A gyrator circuit is constructed such that the conversion factor of the gyrator, and hence the resonant frequency of a tuned circuit, is a function of the transconductances of the bipolar transistors. The circuit allows the resonant frequency to be varied over several octaves by means of an accurately predetermined voltage-frequency relationship.

Resistorless Shenoi Gyrator

The small-signal model of the Shenoi gyrator [1], as shown in Fig. 1, has the following short-circuit admittance parameters:

$$y_{11} = 0, \quad y_{22} = 0, \quad y_{12} = \frac{1}{R_1}, \quad y_{21} = \frac{1}{R_2}$$  (1)

where it is assumed that the transistors are ideal, that is, each transistor behaves as an infinite-gain controlled source ($\beta = \infty, g_m = \infty$). It is well known [1], [4] that the gyrator may be used to simulate a grounded inductance at port 1 by terminating port 2 with a capacitor $C$. In this case, the admittance at port 1 is given by

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The purpose of this correspondence is to consider the behavior of the Shenoi gyrator under the following special conditions: 1) the transistors exhibit low-valued transconductances $g_m$, 2) the interconnecting resistors, $R_1$ and $R_2$, are eliminated by reducing them to zero. It will be shown that, under these conditions, the conversion factor of the gyrator may be controlled by means of a controlling voltage, and that an accurate voltage-tunable resonant circuit may be designed.

The nullor [2], [3] model of a bipolar transistor with infinite $\beta$ and finite low-valued $g_m$ is given in Fig. 2(a) from which it follows that Fig. 2(b) represents a three-nullor model of the Shenoi gyrator where the transconductance terms $g_{m1}$, $g_{m2}$, and $g_{m3}$ appear as additional resistors in series with $R_1$ or $R_2$. The modified conversion factor is therefore given by

$$K = \left[ \frac{1}{R_1 + 1/g_{m1}} \right] \left[ \frac{1}{R_2 + 1/g_{m2} + 1/g_{m3}} \right].$$

For the purpose of this correspondence, $R_1$ and $R_2$ may be equal to zero, thereby obtaining the resistorless Shenoi gyrator in Fig. 3(a) with the conversion factor

$$K = \left[ g_{m1} \right] \left[ \frac{1}{1/g_{m2} + 1/g_{m3}} \right].$$

The transconductance terms $g_{m1}$, $g_{m2}$, and $g_{m3}$ are accurately controllable by means of the transistor emitter bias currents $I_{E1}$, $I_{E2}$, and $I_{E3}$ via the well-known relationship

$$g_m = \frac{2}{kT} |I_E|.$$
The effective inductance at port 1 is given by
\[ L_{eq} = K_0 C_2 = \left| g_m \right| \frac{1}{\left( 1/g_{m2} + 1/g_{m3} \right)} g C_2 \]
and the resonant frequency by
\[ f_0 = \frac{1}{2 \pi \sqrt{L_{eq} C}} = \frac{1}{2 \pi \sqrt{C_1 C_2}} \left[ g_m \left( \frac{1}{1/g_{m2} + 1/g_{m3}} \right) \right]^{1/2}. \]

Thus, substituting (6) and (4) into (5) gives
\[ f_0 = \frac{q}{2 k T \sqrt{C_1 C_2}} \left( \frac{1}{2 I_{E1} + 2 I_{E2}} \right)^{1/2} \]
where \( I_{E1}, I_{E2}, \) and \( I_{E3} \) are easily written in terms of the circuit parameters of Fig. 4 as follows:
\[ I_{E2} = \frac{V_{EB1}}{R_A}; \quad I_{E3} = \left( \frac{E_1 - V_{EB2}}{R_B} \right) - I_{E1}, \quad I_{E3} = \frac{E_2}{R_C}. \]

Thus, varying \( E_0 \) will cause corresponding variations of \( I_{E1}, I_{E2}, \) and therefore of \( f_0 \). It is preferable to select \( C_1 \) and \( C_2 \) such that [4]
\[ \frac{C_1}{C_2} \approx \frac{R_C}{R_A} \]
in order to ensure the maximum \( Q \) factor of the circuit. The parameter values used in Fig. 4 were measured as follows:
\[ V_{EB1} = 0.59 \text{ V}; \quad V_{EB2} = V_{EB1} = 1.02 \text{ V}; \quad R_A = 6.1 \text{ k}\Omega; \quad R_B = 52 \text{ k}\Omega; \quad R_C = 150 \text{ k}\Omega; \quad E_1 = +10.0 \text{ V}; \quad C_1 = 0.974 \mu\text{F}; \quad C_2 = 0.0500 \mu\text{F}; \]
and it was assumed that \( k T/q = 25.0 \text{ mV} \). These experimental values were substituted into (7) and (8) to obtain the theoretical variation of \( f_0 \) as a function of the tuning voltage \( E_0 \). The resultant theoretical frequency–voltage characteristic is given, with the measured characteristic, in Fig. 5. Note that good agreement (better than 2\% percent) is obtained for a frequency variation from 550 to 2600 Hz, corresponding to a tuning voltage \( E_0 \) varying from -7.0 to -30.0 V. Reducing \( C_1 \) and \( C_2 \) by a factor of 10 allowed a similar characteristic to be obtained over the frequency range of 5500 to 26000 Hz.

It should be noted from (7) that \( f_0 \) is inversely proportional to absolute temperature \( T \). Thus,
\[ S_T f_0 = -1. \]

This sensitivity of the resonant frequency to temperature variations is due to the inherent temperature dependence of \( g_m \) and, in some applications, may be a practical limitation of this circuit.

The circuit is capable of handling signal voltage amplitudes of approximately 100 mV, beyond which the small signal parameters \( g_m \) vary sufficiently (on a per-cycle basis) to cause noticeable distortion. There does not appear to be any reason for preventing the fabrication of the circuit in microelectronic form. It is particularly useful where moderate selectivity (10

One-Phase CCD: A New Approach to Charge-Coupled Device Clocking

R. D. MELEEN AND JAMES D. MEINDL

Abstract—A new approach to charge-coupled device (CCD) clocking has been developed that uses a single clock signal and dc bias on a device structure previously used for two-phase clocking. The one-phase approach results in improved operation by simplifying the clock circuit, reducing power consumption, and simplifying scanning of large CCD arrays.

To date, three different techniques have been described for control of charge shifting in charge-coupled devices (CCD) [1]–[3]. They are commonly referred to as two-phase, three-phase, and four-phase techniques. These techniques all suffer to varying degrees from requirements for complex clocks and many clock lines. The new technique to be discussed here significantly reduces these complex clocking requirements by using only one clocking signal. This is a large reduction in complexity of the clocking circuitry because there is no requirement for pulses on different clock lines to overlap.

This one-phase technique may be used with the CCD device structure shown in Fig. 1. This structure is identical to that used in two-phase charge-coupled techniques that achieve directionality of charge motion by a gradient in the surface potential due to a step in the thin silicon oxide between the semiconductor surface and the CCD plate [1]. In the two-phase technique overlapping clock pulses such as shown in Fig. 2(a) are applied to the two clock lines. The new one-phase technique uses a dc bias on one clock line and a pulsing clock on

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