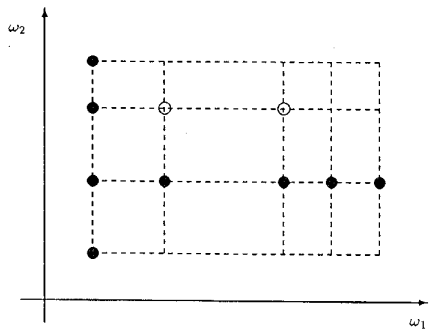

Fig. 2. Constellation of 2-D frequencies that satisfy the condition of Corollary 1.

and, hence, we have

$$\text{rank}\left(\begin{bmatrix}\lambda I - A \\ C\end{bmatrix}\right) = \text{rank}\left(\begin{bmatrix}D_1 & 0 \\ 0 & 0 \\ V_1 & V_2\end{bmatrix}\right) = \text{rank}(D_1) + \text{rank}(V_2)$$

where $D_1 = \text{diag}(y_i - y'_1, \cdots, y_i - y'_{N_s-m})$, $V_2 = V[(z'_1, \cdots, z'_m)^T, L]$, none of $\{y'_1, \cdots, y'_{N_s-m}\} \subset \{y_1, \cdots, y_{N_s}\}$ is equal to y_i, and the poles in $\{z'_1, \cdots, z'_m\} \subset \{z_1, \cdots, z_{N_s}\}$ are distinct. So the rank of D_1 is $N_s - m$. The rank of V_2 is m iff $L \geq m$. Hence, rank $([{}^{\lambda I - A}_{C}]) = N_s$ for $\lambda = y_i$ iff $L \geq m$. Therefore, rank $([{}^{\lambda I - A}_{C}]) = N_s$ for all $\lambda \in \{y_i\}$ iff $L \geq m_y$. Since A has d_y distinct diagonal elements, the order of the minimum polynomial of A is equal to d_y. So, by Lemma 1, for $K \geq d_y$, rank $[E_l(K, L)] = N_s$ iff $L \geq m_y$.

We can symmetrically get the other half conclusion of (a) by using the fact that there exists a permutation matrix P [2] such that

$$PE_l = \begin{bmatrix} V(y, K) \\ V(y, K)Z_d \\ \vdots \\ V(y, K)Z_d^{L-1} \end{bmatrix} = O_L[V(y, K), Z_d] \tag{5}$$

where $y \hat{=} (y_1, \cdots, y_{N_s})^T$ and $Z_d = \text{diag}(z_1, \cdots, z_{N_s})$.

Part (b) follows readily from part (a) since $E_r = E_l^T(M - K + 1, N - L + 1)$.

From (2), we know that rank $(X_e) = N_s$ iff rank $(E_l) =$ rank $(E_r) = N_s$. Combining (a) and (b), we have (c). Q.E.D.

Theorem 2:

1) rank $[E_l(K, L)] < N_s$ if $L < m_y$ or $K < m_z$.
2) rank $[E_r(K, L)] < N_s$ if $L > N - m_y + 1$ or $K > M - m_z + 1$.
3) rank $[X_e(K, L)] < N_s$ if $L < m_y$ or $K < m_z$ or $L > N - m_y + 1$ or $K > M - m_z + 1$.

Proof: Following the first paragraph of the proof for Theorem 1, one can show that if $\lambda = y_i$ that has the maximum multiplicity m_y, then rank $(V_2) < m_y$ if $L < m_y$ and hence rank $([{}^{\lambda I - A}_{C}]) < N_s$ if $L < m_y$. Therefore, by Lemma 2, rank $[E_l(K, L)] < N_s$ if $L < m_y$. Other proofs can be done similarly. Q.E.D.

By Theorems 1 and 2, the whole window size set $G = \{(K, L): 1 \leq K \leq M, 1 \leq L \leq N\}$ is divided into three sets $G = G_0 \cup G_1 \cup G_u$ (see Fig. 1). For the sets G_0 and G_1, we have definite answers: i.e., rank $[X_e(K, L)] < N_s$ when $(K, L) \in G_0$, and rank $[X_e(K, L)] = N_s$ when $(K, L) \in G_1$. But for G_u, the answer is uncertain depending on the distribution of the signal poles. In other words, rank $[X_e(K, L)]$ may be less than or equal to N_s for $(K, L) \in G_u$. It should be noted that the sufficient condition given in [2], i.e., $N_s \leq K \leq M - N_s + 1$ and $N_s \leq L \leq N - N_s + 1$, is a subset of G_1.

When $m_y = d_z$ and $m_z = d_y$, the set G_u is empty. From Theorems 1 and 2, we have the following sufficient and necessary constraint on the window size under which the rank of the enhanced data matrix is equal to the desired number.

Corollary 1: If $m_y = d_z$ and $m_z = d_y$, then

$$\text{rank}[X_e(K, L)] = N_s \text{ iff } d_y \leq K \leq M - d_y + 1, \quad d_z \leq L \leq N - d_z + 1.$$

Note that the condition of Corollary 1 is satisfied when all 2-D frequencies are scattered on a rectangular grid (not necessarily uniform) and at least one straight line in each dimension on the grid is fully occupied by 2-D frequencies, which is illustrated in Fig. 2.

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High-Speed Systolic Ladder Structures for Multidimensional Recursive Digital Filters

Xiaojian Liu and Leonard T. Bruton

***Abstract*—We propose a multilevel approach for designing high-speed systolic ladder structures for multidimensional (MD) recursive digital filters. Based on appropriately selected 1-D filter structures for each filter dimension (or level), a large variety of MD systolic filter structures may be derived. In particular, we introduce a new 1-D filter structure that proves the most suitable structure in terms of a systolic ladder implementation, because it leads to MD ladder filter structures possessing such important properties as the shortest critical path (for filters without order augmentation), the canonic number of high-level storage registers (e.g., line and frame registers of images), and local interconnectivity.**

I. INTRODUCTION

High-speed multidimensional (MD) digital filtering is very useful for real-time video signal processing such as video image coding, bandwidth compression, sampling rate conversion and the enhancement of television signals. In this contribution, we are concerned

Manuscript received March 16, 1993; revised August 22, 1995. The associate editor coordinating the review of this manuscript and approving it for publication was Prof. Russell M. Mersereau.

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Publisher Item Identifier S 1053-587X(96)02273-6.

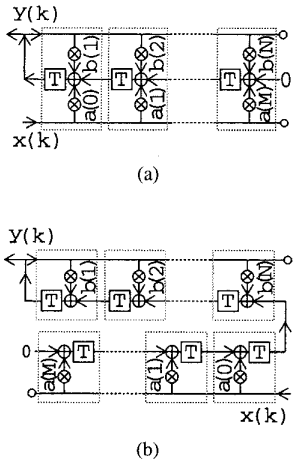

Fig. 1. Well-known 1-D filter structures. (a) Canonic number of shift register structure $S1$. (b) Improved modularity structure $S2$.

with the systolic implementation of real-time MD recursive digital filters, which provides a high level of computational parallelism, local interconnectivity, modularity, and regularity.

Real-time systolic implementations of MD recursive digital filters have been discussed in prior work [1]–[8]. However, prior work has concentrated either on minimizing the critical path (that is, the unlatched signal path that requires the longest processing time) [1], [2] or on achieving the modularity and regularity of filter structures [3]–[8]. Thus, the previously proposed filter structures do not satisfy the practical requirement of simultaneously having a critical path containing no more than one multiplier and one adder and the desired modularity and regularity. Moreover, they do not provide the property of local interconnectivity, which is essential in deep submicron VLSI implementations. In this contribution, we propose a new 1-D ladder filter structure, based on which we introduce a multilevel approach to derive MD ladder filter structures that are regular, modular, and locally interconnected on the one hand, and yet have the shortest critical path of one multiplier plus one adder and the canonic number of storage registers in the higher dimensions (e.g., image line and frame registers).

Appropriate 1-D filter structures are essential in the proposed multilevel approach because they determine many characteristics of the derived MD filter structures. In the following, we first introduce a new and useful 1-D systolic filter structure together with its derived forms in Section II, then propose high-speed MD systolic ladder filter structures in Section III.

II. New 1-D Filter Structures

It is known that an n-dimensional (n-D and n is a positive integer) recursive digital filter can be considered as a 1-D recursive block filter whose coefficients are not constants but are certain $(n-1)$-D nonrecursive filter transfer functions. Each of these $(n-1)$-D nonrecursive filters can be considered again as a 1-D nonrecursive block filter whose coefficients are $(n-2)$-D nonrecursive filter transfer functions, and so forth. In this way, we can decompose an n-D filter to an n-level block filter.

For the MD systolic ladder filter structures proposed in the next section, two 1-D block filter structures are used for the n to $(n-1)$ upper level block filters. These 1-D block filter structures are derived from well-known 1-D filter structures shown in Figs. 1(a) and (b), where we employ three-input adders to reduce the complexity of the diagrams. We refer here to these 1-D filter structures as structure $S1$ and $S2$, respectively, where the corresponding difference equation is

$$y(k) = \sum_{i=0}^{M} a(i)x(k-i) + \sum_{i=1}^{N} b(i)y(k-i) \tag{1}$$

where $x(k)$ and $y(k)$ are the input and output signals, $a(i)$ and $b(i)$ are constant coefficients, and M and N are the degrees of the nonrecursive and the recursive filter parts, respectively.

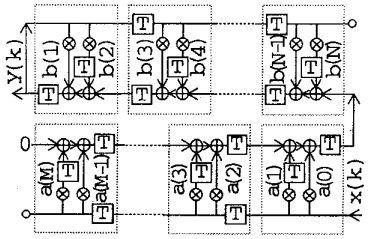

Fig. 2. Proposed new 1-D systolic filter structure $S3$.

The first and the lowest filter level is not a block filter but an embedded 1-D filter. For this first filter level, all the previously known 1-D filter structures are not maximally suitable, because they do not satisfy the requirement of simultaneously possessing such properties as regularity (in particular, a cascade of uniform *processing elements* (PE's)), modularity (i.e., simple PE's), the shortest critical path and the local interconnectivity of PE's. These properties are the most critical requirements for a practical useful MD systolic filter structure. In order to satisfy all the above-mentioned properties, a new 1-D filter structure is proposed.

Reconsidering the $S2$ structure in Fig. 1(b), we group two multiplier coefficients into a new single PE and cascade the PE's in a similar way such as shown in structure $S2$. The resulting 1-D filter structure is shown in Fig. 2. We refer to this new filter structure as the $S3$ structure. It is easily verified that the critical path of structure $S3$ involves just one multiplier and one adder and that the global interconnections are interrupted.

The input of the $S3$ filter structure is delayed by $\langle N/2 \rangle + 1$ processing periods (referred to here as the input latency of the structure), where $\langle \cdot \rangle$ stands for the integer part. To lower this latency and especially to share shift registers, the recursive and nonrecursive parts are implemented together in the filter structure $S4$ shown in Fig. 3(a), where three-input adders are again used to reduce the complexity of the diagram. This filter structure has no input latency and a smaller number of shift registers but a longer critical path compared with structure $S3$. However, the dual structure of $S4$, which is shown in Fig. 3(b) and referred to as the $S5$ structure, has the same minimal critical path as structure $S3$, and the input latency can be shortened by inserting the input signal next to the multiplier $b(2)$.

All the 1-D filter structures $S3$ to $S5$ do not have the minimal number of shift registers. However, because these structures will be embedded in the lowest level of an MD filter structure, the corresponding shift registers are pixel registers, whose number we allow to be noncanonic (cf. Section III).

III. MD Ladder Filter Structures

The 1-D filter structures discussed above are now used to realize MD filter structures. The proposed approach of constructing MD filter structures is not limited to employing the proposed 1-D filter structures. The variety of suitable 1-D filter structures may lead to a variety of useful MD systolic filter structures.

Let us consider the 3-D recursive filter described by the difference equation

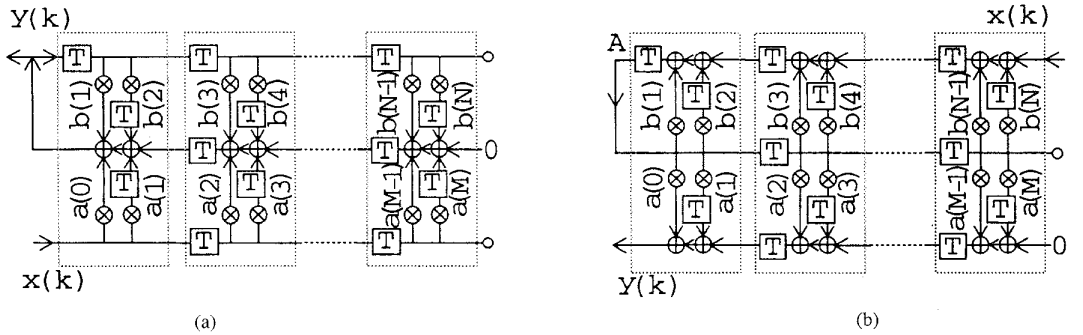

Fig. 3. Derived forms of the proposed 1-D filter structure. (a) Minimized number of shift registers structure $S4$. (b) Minimized critical path structure $S5$.

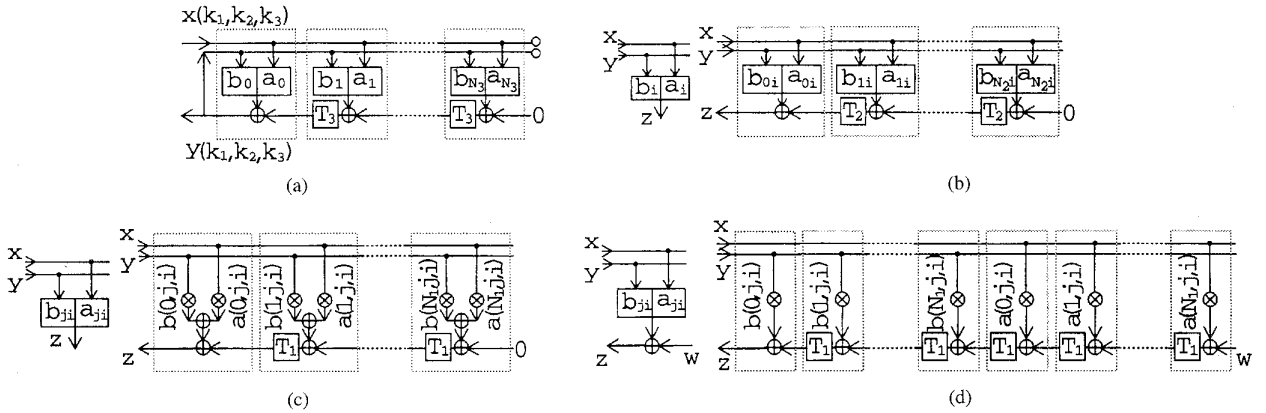

Fig. 4. Examples in Section III-A. (a) Third-level block structure. (b) Second-level block structure. (c) First-level structure of Structure $S1$-$S1$-$S1$; (d) first-level structure of Structure $S1$-$S1$-$S2$.

$$
\begin{aligned}
&y(k_1,k_2,k_3)\\
&\quad=\sum_{i_1=0}^{N_1}\sum_{i_2=0}^{N_2}\sum_{i_3=0}^{N_3} a(i_1,i_2,i_3)x(k_1-i_1,k_2-i_2,k_3-i_3)\\
&\qquad+\sum_{\substack{i_1=0\\ i_i\neq i_2\neq i_3\neq 0}}^{N_1}\sum_{i_2=0}^{N_2}\sum_{i_3=0}^{N_3} b(i_1,i_2,i_3)y(k_1-i_1,k_2-i_2,k_3-i_3).
\end{aligned}
\tag{2}
$$

Assume that k_1 and k_2 are the two spatial coordinates and k_3 is the temporal coordinate. The unit shift operations in the k_3, k_2, and k_1 directions imply the storage of one image frame, one image line and one image pixel, respectively. Assume that an image frame has a size of $K \times K$ pixels. Then, the frame register T_3, the line register T_2, and the pixel register T_1 contain $K \times K$, K and one image pixel(s), respectively. Thus, the relationship between the sizes of storage registers T_1 to T_3 is

$$T_3 = K^2 T_1 = K T_2. \tag{3}$$

Since the T_3 and T_2 registers are much bigger than the T_1 registers, the number of T_3 and T_2 registers have to be kept canonic, whereas a greater than canonic number of the much smaller T_1 registers may be chosen to achieve other structural features such as local interconnections and short critical paths.

Hereafter, we describe the proposed multilevel approach by considering three 3-D examples. The first example is an especially simple example. The filter structures derived in this example contain signal broadcasts; in the strict sense they are not systolic structures. However, because of the simplicity of this example, it provides insight into the proposed multilevel approach.

A. Simple Examples: Structures $S1$-$S1$-$S1$ and $S1$-$S1$-$S2$

We modify the 1-D structure $S1$ to a 1-D *block* structure given in Fig. 4(a), implementing the third (uppermost) level of the 3-D filter given by (2), because we want to minimize the frame registers T_3 to the canonic number. The blocks $(a_i, b_i)\,(i = 0, 1, 2, \ldots)$ in Fig. 4(a) denote the lower (second) level structures, and the symbols a_i and b_i denote the set of filter coefficients $a(i_1, i_2, i_3)$ and $b(i_1, i_2, i_3)$, whose third indices i_3 are uniformly equal to i.

Also, to minimize the number of line registers T_2, we use the 1-D canonic structure $S1$ for the second filter level. That is, the blocks in Fig. 4(a) are given by the second-level block structure in Fig. 4(b), where the blocks (a_{ji}, b_{ji}) denote the lower (first) level structures. The symbols a_{ji} and b_{ji} denote the set of filter coefficients $a(i_1, i_2, i_3)$ and $b(i_1, i_2, i_3)$ whose second and third indices i_2 and i_3 are uniformly j and i, respectively.

For the lowest (first) filter level, we again use (for the purpose of explanation) the 1-D canonic structure $S1$. That is, the blocks in Fig. 4(b) are given by the first-level structure in Fig. 4(c).

Putting the first-level structure in Fig. 4(c) into the second-level block structure in Fig. 4(b), we obtain the 2-D second-level *complete* structure in Fig. 5(a). The final 3-D structure shown in Fig. 5(b) is obtained by replacing the second-level blocks in Fig. 4(a) by the second-level complete structure in Fig. 5(a). This structure is called Structure $S1$-$S1$-$S1$, indicating the three 1-D structures used for three different filter levels.

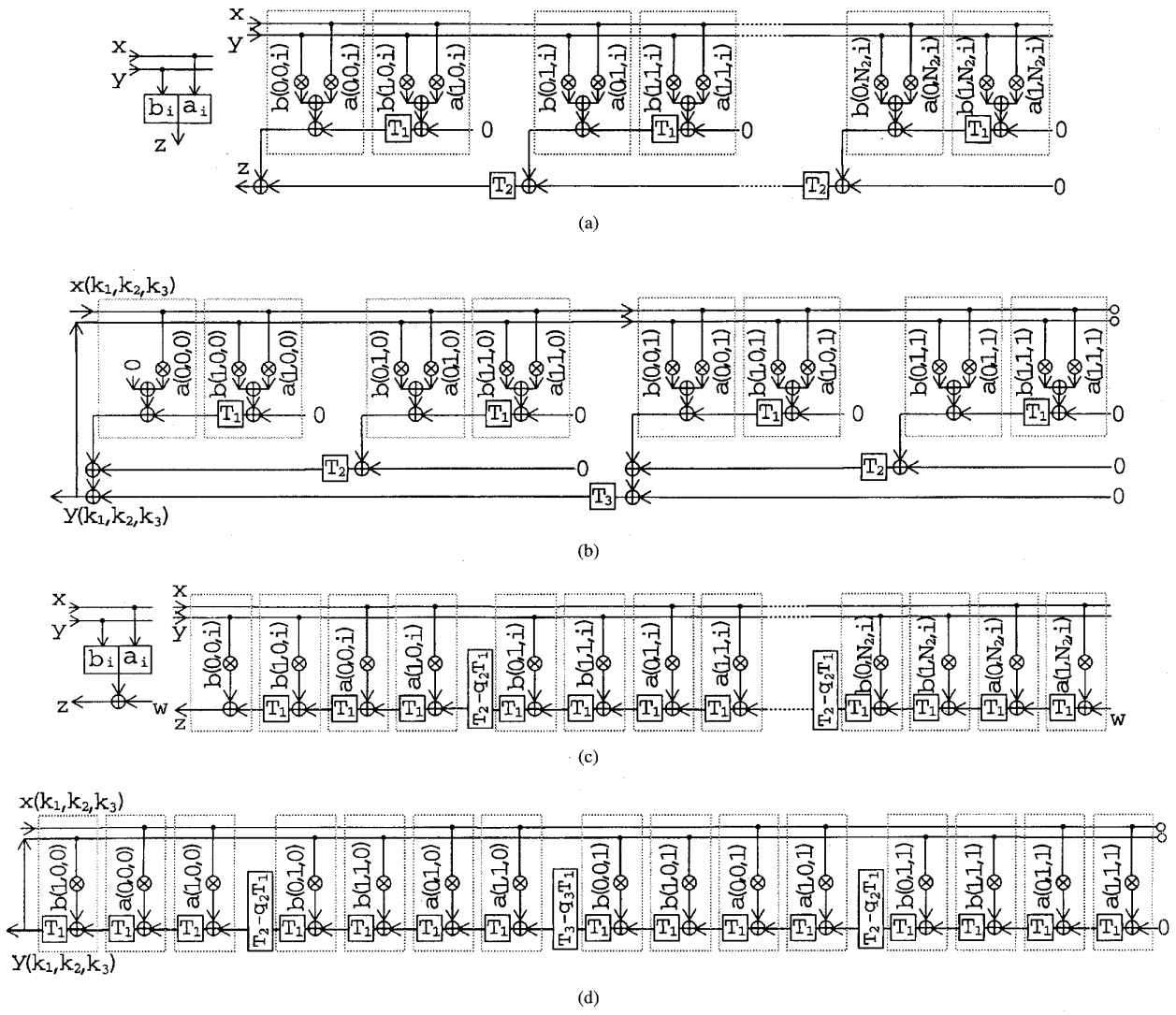

Fig. 5. Examples in Section III-A. (a) Second-level complete structure of Structure $S1$-$S1$-$S1$ ($N_1 = 1$). (b) Third-level complete structure of Structure $S1$-$S1$-$S1$ for $N_1 = N_2 = N_3 = 1$. (c) Second-level complete structure of Structure $S1$-$S1$-$S2$ ($N_1 = 1$). (d) Third-level complete structure of Structure $S1$-$S1$-$S2$ for $N_1 = N_2 = N_3 = 1$.

The construction of the above filter structure is very simple, and the obtained structure is quite modular and regular. However, it has global interconnections, and the critical path is two multipliers plus seven adders.

The critical path can be reduced to one multiplier plus one adder by using 1-D minimized critical path structures such as Structure $S2$ shown again in Fig. 4(d) for the first filter level. This first-level structure has a critical path of one multiplier plus one adder and an input latency of $N_1 + 1$ processing periods. In this new approach, the adder next to a block symbol (cf. Fig. 4(d)) is also included in the first-level structure to improve the regularity.

Putting the first-level structure in Fig. 4(d) into the second-level block structure in Fig. 4(b), we obtain the 2-D second-level complete structure in Fig. 5(c). Since we have included the adder into the first-level structure as shown in Fig. 4(d), the pixel registers of a particular first-level structure affect the signal delays of the first-level structures located before it. In order to compensate this effect and to maintain the validity of (2) for the obtained higher level complete structure (within a constant input latency), the line register T_2 is replaced by $T_2 - q_2T_1$, where the equivalence formula (3) between the storage registers T_1 to T_3 has been employed. Among the q_2 pixel registers T_1 that are subtracted from a line register T_2, $q_2 - 1$ are to balance the number of the pixel registers T_1 in the lower path of the first-level structure, that is (for $M_1 = N_1$),

$$q_2 - 1 = 2N_1 + 1 \tag{4}$$

and the remaining one is to balance the pixel register T_1 that is inserted in front of the first-level structure.

Putting the second-level complete structure in Fig. 5(c) into the third-level block structure in Fig. 4(a), we obtain the 3-D third-level complete structure $S1$-$S1$-$S2$ in Fig. 5(d). Again, to adjust the number of storage registers introduced by inserting the second-level complete structure, the frame register T_3 is replaced by $T_3 - q_3T_1$. The integer $q_3 - 1$ is the number of the pixel registers in lower path of the second-level complete structure, that is (for $M_2 = N_2$),

$$q_3 - 1 = N_2K + q_2 - 1. \tag{5}$$

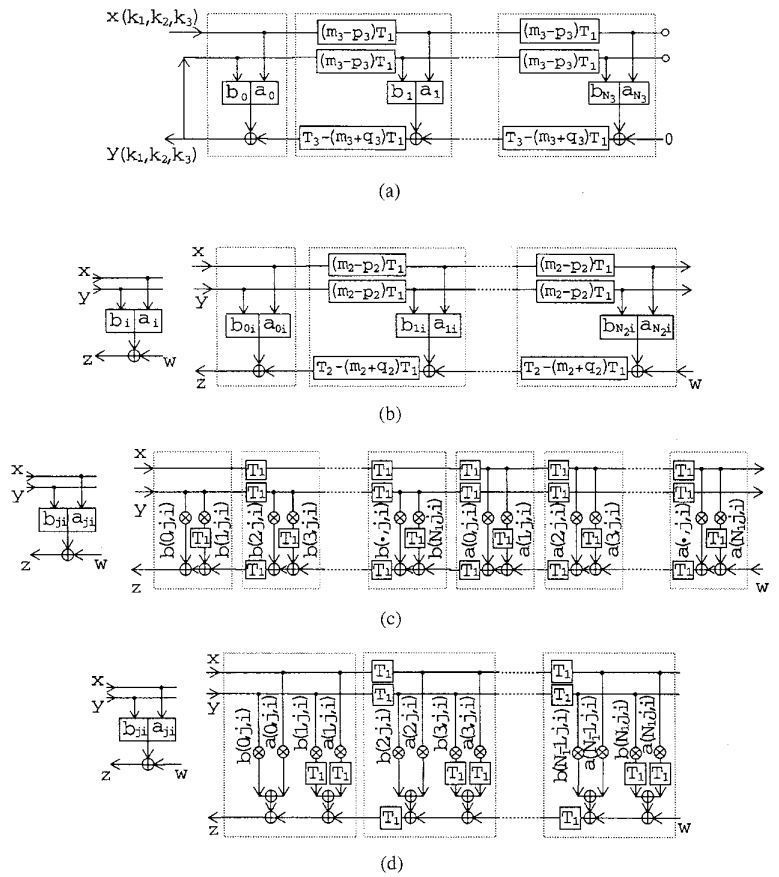

Fig. 6. Examples in Section III-B. (a) Third-level block structure. (b) Second-level block structure. (c) First-level structure of Structure $S1$-$S1$-$S3$. (d) First-level structure of Structure $S1$-$S1$-$S4$.

B. Systolic Ladder Structure $S1$-$S1$-$S3$ and the Dual of Structure $S1$-$S1$-$S4$

As is seen in Fig. 5, the structures in the above example contain global interconnections, which may lengthen the critical path and increase the load on the input signal as the number of multiplier coefficients increases. These global interconnections can, however, be interrupted by using a modified 1-D canonic block structure for the upper filter levels. In fact, we modify the 1-D third-level block structure in Fig. 4(a) to the block structure in Fig. 6(a), where the previous global interconnections have been interrupted by shifting a small number of pixel registers $(m_3 - p_3)T_1$ contained in the frame registers T_3, into the input and output data bus, respectively. The integers p_3 and q_3 are provisionally equal to zero, and the integer m_3 can be chosen equal to one so that the structure in Fig. 6(a) only has an increase of N_3 pixel registers compared with the original canonic structure in Fig. 4(a). For the convenience of later discussion, we maintain the notation of the integer expression $m_3 - p_3$ and $m_3 + q_3$ in the structure.

Also, we use the above modified 1-D canonic structure for the second filter level. That is, the blocks in the third-level structure in Fig. 6(a) are implemented by the second-level block structure in the way shown in Fig. 6(b), where the integer p_2 and q_2 are provisionally equal to zero and the integer m_2 can be chosen equal to one.

For the first filter level, we cannot use the modified 1-D canonic filter structure, because the global interconnection cannot be removed on this level in the same manner as above. Therefore, we employ the 1-D $S3$ structure shown again in Fig. 6(c), which does not contain global interconnections and has a critical path of one multiplier plus one adder. The input latency of this structure is $2(\langle N_1/2\rangle + 1)$.

Putting the first-level structure in Fig. 6(c) into the second-level block structure in Fig. 6(b) and putting the obtained second-level complete structure shown in Fig. 7(a) into the third-level block structure in Fig. 6(a), we obtain the 3-D third-level complete structure $S1$-$S1$-$S3$ in Fig. 7(b). Similar to what is discussed in Section 3.1, the parameters p_i and q_i $(i = 2, 3)$ are used to balance the number of the pixel registers T_1 in the upper and lower path of the first-level structures, respectively. m_i $(i = 2, 3)$ are now chosen to achieve a regular PE. These parameters are now given by

$$p_2 = 2\langle N_1/2\rangle + 1, q_2 = m_2 = p_2 + 1, \quad \text{(6a, b, c)}$$

$$p_3 = N_2 m_2 + p_2, \quad q_3 = N_2(K - m_2) + q_2, \quad m_3 = p_3 + 1. \quad \text{(7a, b, c)}$$

Note that in Fig. 7(a) and 7(b) the PE's containing the a and b coefficients are abbreviated to rectangular boxes with the a and b coefficients, respectively, and the pixel register T_1 before the multiplier $b(1, 0, 0)$ in Fig. 7(b) is shifted behind it so that all the multipliers are clocked at the same time instant.

The $S1$-$S1$-$S3$ structure in Fig. 7(b) is a highly systolic ladder structure, where all the PE's marked by rectangles are locally interconnected, the critical path is just one multiplier plus one adder and the numbers of line and frame registers T_2 and T_3 are canonic, respectively, implying minimal chip area.

Using the above approach, we can derive a number of MD systolic ladder structures. For example, the input latency of Structure

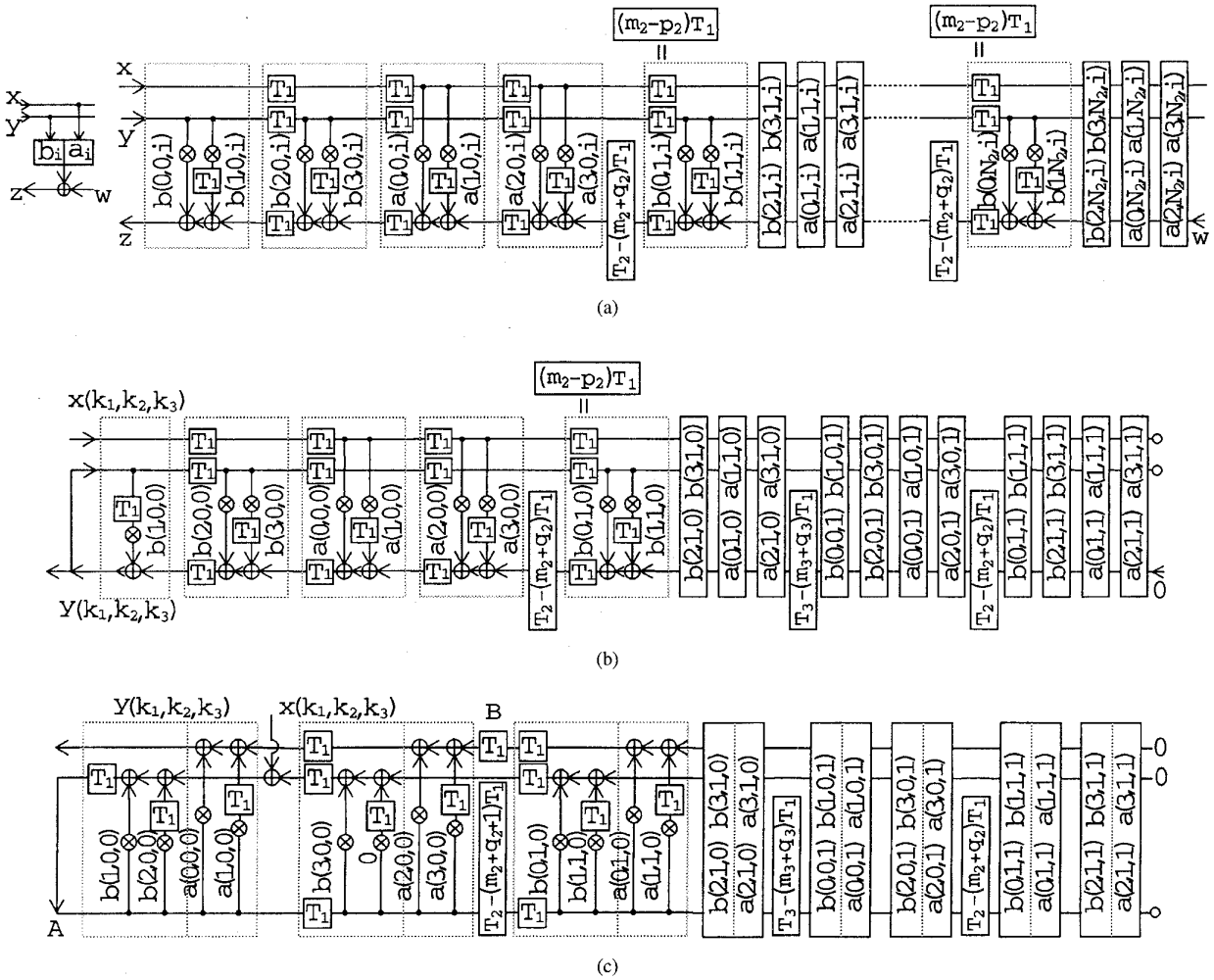

Fig. 7. Examples in Section III-B. (a) Second-level complete structure of Structure $S1$-$S1$-$S3$ ($N_1 = 3$). (b) Third-level complete structure of Structure $S1$-$S1$-$S3$ for $N_1 = 3$, $N_2 = N_3 = 1$. (c) Third-level complete structure of the dual Structure $S1$-$S1$-$S4$ for $N_1 = 3$, $N_2 = N_3 = 1$.

$S1$-$S1$-$S3$ can be avoided by employing Structure $S4$ given in Fig. 6(d) for the first filter level. Putting the first-level structure in Fig. 6(d) into the second-level block structure in Fig. 6(b) and putting the obtained second-level complete structure into the third-level block structure, we obtain the 3-D third-level complete Structure $S1$-$S1$-$S4$, where the parameters p_i, q_i and m_i $(i = 2, 3)$ are given by the same formulas as in (6) and (7) except for $p_2 = \langle N_1/2 \rangle$. The desired final structure is the dual structure of Structure $S1$-$S1$-$S4$ given in Fig. 7(c), where an additional pixel register T_1 is inserted in the place B, in order to balance the pixel register T_1 next to the multiplier $b(1, 0, 0)$ in the first PE. These two pixel registers are considered in the first line register so that it becomes $T_2 - (m_2 + q_2 + 1)T_1$ instead of $T_2 - (m_2 + q_2)T_1$. This new structure has an input latency of just one period and a critical path of one multiplier plus one adder. Also, note that the first-level structure involved in the above dual structure is the structure $S5$ in Fig. 3(b).

C. Systolic Ladder Structure $S2$-$S2$-$S3$ With Improved Modularity

If the frame and line registers are not realized on-chip, we can allow structures that are noncanonic in the number of registers to be used for the upper filter levels. Using the resulting freedom for the upper level filter structures, we improve the modularity of the final ladder structures.

For example, we modify the 1-D structure $S2$ to the third- and second-level block structure in Figs. 8(a) and 8(b). For the first filter level, we use Structure $S3$ in Fig. 8(c). Putting the first-level structure in Fig. 8(c) into the second-level block structure in Fig. 8(b) and putting the obtained second-level complete structure in Fig. 9(a) into the third-level block structure in Fig. 8(a), we obtain the third-level complete structure $S2$-$S2$-$S3$ shown in Fig. 9(b), where the parameters p_i, q_i and m_i $(i = 2, 3)$ are given by the same formulas as in (6) and (7) except for $p_2 = \langle N_1/2 \rangle$.

IV. Concluding Remarks

We have proposed a new and useful 1-D systolic filter structure, based on which we have derived a class of MD systolic ladder filter structures, that are highly regular, modular, locally interconnected and have a critical path of one multiplier plus one adder. It can be shown that with little additional circuitry the zero boundary condition can be ensured for all the structures.

Since the proposed MD systolic ladder filter structures are locally interconnected, the interconnect delay and buffering delay are kept minimum. The critical path of the filter circuit is essentially the processing time of one multiplication and one addition. Using current VLSI technology, we are able to implement a programmable 16×12-b multiplication plus a 16–b addition in less than 25 ns or

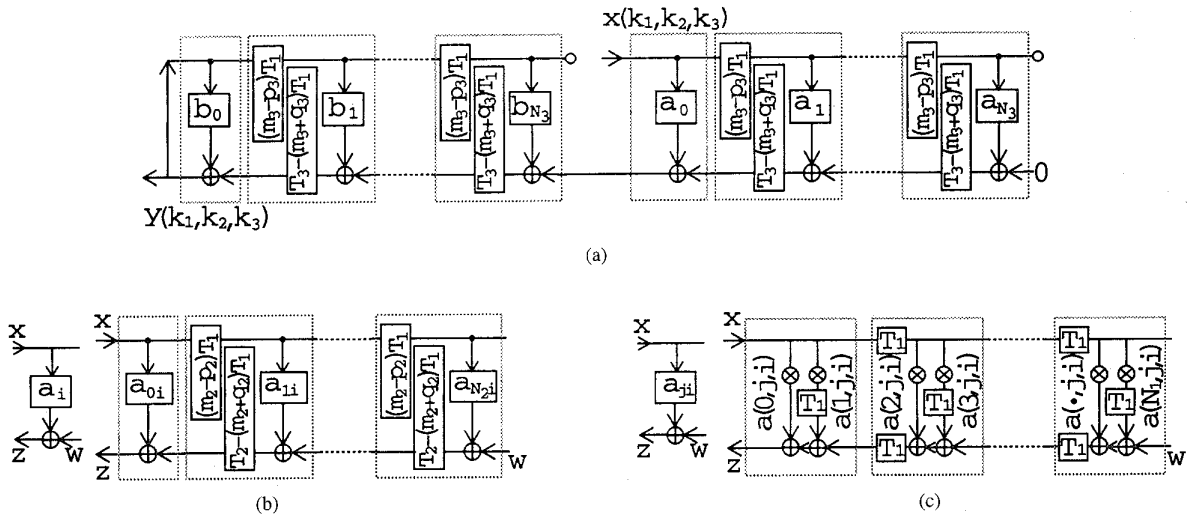

Fig. 8. Examples in Section III-C. (a) Third-level block structure. (b) Second-level block structure. (c) First-level structure of Structure $S2$-$S2$-$S3$.

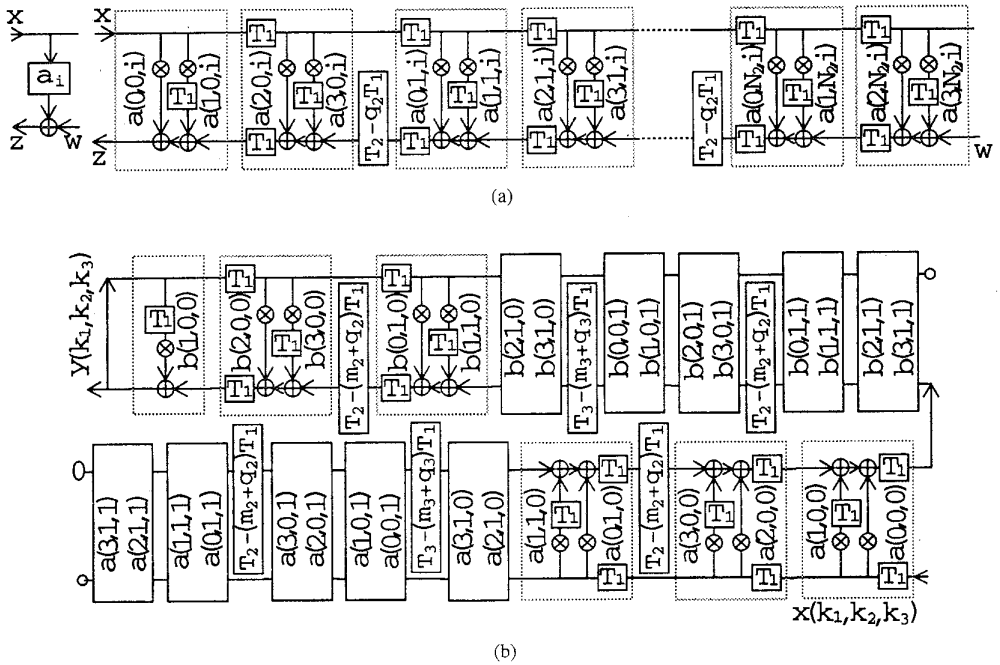

Fig. 9. Examples in Section III-C. (a) Second-level complete structure of Structure $S2$-$S2$-$S3$ ($N_1 = 3$). (b) Third-level complete structure of Structure $S2$-$S2$-$S3$ for $N_1 = 3$, $N_2 = N_3 = 1$.

faster than 40 MHz. The current CCIR and SMPTE digital video standards set a video pixel frequency of 13.5 MHz or 18 MHz for wide screen. Therefore, the proposed MD filter structures can well accommodate the real-time processing of current digital video signals.

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Correction to "A Capon's Time-Octave Representation Application in Room Acoustics"

In [1], on pages 1851 and 1852, the captions for Figs. 6 and 7 are correct, but the figures should be exchanged. In addition, on page 1851 on the third line of the left-hand column, "Fig. 7" should read "Fig. 5."

REFERENCES

[1] N. Martin, J. Mars, J. Martin, and C. Chorier, "A Capon's Time-Octave Representation Application in Room Acoustics," *IEEE Trans. Signal Processing*, vol. 43, no. 8, pp. 1842–1854, Aug. 1995.